**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Filing Date: | Unknown | ) |
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| Priority Date: | 15 November 2000 | ) |
| | | ) |
| Applicants: | BROADHURST, Denzil | ) |
| | | ) |
| For: | SIGNAL SEQUENCING CONTROL MEANS | ) |

**PRELIMINARY AMENDMENT**

Director For Patents
Box: New Application
Washington, D.C. 20231

Dear Sir:

This is a preliminary amendment to the enclosed application entitled "Signal Sequencing Control Means" claiming priority to British Patent Application No. 0027810.1 filed 15 November 2000.

In the Specification:

Please amend the specification as follows:

Page 1, after the title, insert the following headers and paragraph:

**--CROSS-REFERENCE TO RELATED APPLICATION**

This application claims priority to British Patent Application 0027810.1 filed 15 November 2000.

**BACKGROUND OF THE INVENTION–**

Page 2, before line 7, insert the Header:

**--SUMMARY OF THE INVENTION–**

Page 4, before line 24 insert the following header:

**--BRIEF DESCRIPTION OF THE DRAWINGS–**

Page 4, before line 27, add the Header:

**--DESCRIPTION OF THE PREFERRED EMBODIMENTS--.**

Page 6 after the last line, insert the following paragraph:

--While the invention has been described with a certain degree of particularly, it is manifest that many changes may be made in the details of construction and the arrangement of components without departing from the spirit and scope of this disclosure. It is understood that the invention is not limited to the embodiments set forth herein for purposes of exemplification, but is to be limited only by the scope of the attached claim or claims, including the full range of equivalency to which each element thereof is entitled.--

**IN THE CLAIMS:**

1. (Amended) A signal sequencing control means for an electronic device, said sequencing control means [including] comprising:

an electronic circuit [(2)] driven to generate the sequence of control signals in a forward and reverse direction along the same circuit path; and

timing means[,] to allow a sequence of control signals to be activated in a pre-determined order for operation of the device and deactivated in a reverse order for disabling the device[, characterised in that the electronic circuit is driven to generate the sequence of control signals in a forward and reverse direction along the same circuit path].

2. (Amended) A signal sequencing control means according to claim 1 [characterised in that] wherein each signal is controlled by a resistor/capacitor combination.

3. (Amended) A signal sequencing control means according to claim 2 [characterised in that] wherein the control signals are controlled by a network of said resistor/capacitor combinations [(18, 20; 24, 26; 30, 32; 18, 38)] and [this] the network provides the activation/deactivation of the signals in sequence at pre-determined time intervals.

4. (Amended) A signal sequencing control means according to claim 3 [characterised in that] wherein the resistors [(18, 24, 30)] of the network are provided in series.

5. (Amended) A signal sequencing control means according to claim 1 [characterised in that the] wherein said sequence of control signals is being operated via [a number of] at least one logic gate[s (14, 22, 28, 34)].

6. (Amended) A signal sequencing control means according to claim 5 [characterised in that one or more of the logic gates (14, 22, 28, 34) are] wherein at least one of said logic gate is a Schmidt Logic Gate[s].

7. (Amended) A signal sequencing control means according to claim 1 [characterised in that] wherein the circuit path includes [one or more logic gates (14, 22, 28, 34)] at least one logic gate and voltage is driven by at least one of said gates along a circuit path through a series of resistors [(18, 24, 30)] in a first direction via a diode [(16)] at the start of the resistor path, and a reverse diode [(36) is] being provided at the end of the resistor path to drive the voltage through the resistors [(18, 24, 30)] in the reverse direction.

8. (Amended) A signal sequencing control means according to claim 1 [characterised in that the] wherein said sequence of signals in a forwards direction is different to the sequence of signals in a reverse direction and the control signals in the forwards and reverse direction is driven using the same circuit path.

9. (Amended) A signal sequencing control means according to claim 1 [characterised in that the] wherein said electronic device is a smart card.

10. (Amended) A signal sequencing control means according to claim 9 [characterised in that the] wherein said smart card has at least three lines [(6, 8, 10)] which need to be activated in a pre-determined order for operation of [the] said device and deactivated in a reverse order for disabling [the] said device.

11. (Amended) A signal sequencing control means for a smart card interface, said interface [including] comprising:

an electronic circuit [(2)] driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path; and

timing means[,] to allow a sequence of control signals to be activated in a pre-determined order for operation of the card and deactivated in a reverse order for disabling the card [and characterised in that the electronic circuit is driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path].

12. (Amended) A smart card reading apparatus, said apparatus for reading/receiving and

processing signals for a smart card, said reading apparatus comprising:[having]

an electronic circuit [(2)] driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path; and [wherein the reading apparatus includes]

a timing means to allow a sequence of control signals to be activated in a pre-determined order for operation of the card and deactivated in a reverse order for disabling the card [and characterised in that the electronic circuit is driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path].

## REMARKS

Attached is the clean version of the claims and new paragraphs as required in Section 1.121(4) (ii).

The application should now be in condition for examination, which is respectfully requested.

Respectfully Submitted

HEAD, JOHNSON & KACHIGIAN

Dated: 11/9/01

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New Header to be Inserted on Page 1, before line 1:

--CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to British Patent Application No. 0027810.1filed 15 November 2000

## BACKGROUND OF THE INVENTION

Header to be inserted into Page 2

## SUMMARY OF THE INVENTION

Headers to be Inserted into Page 4:

## BRIEF DESCRIPTION OF THE DRAWINGS

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

**New Paragraph for Page 6 to be Inserted After the Last Line:**

While the invention has been described with a certain degree of particularly, it is manifest that many changes may be made in the details of construction and the arrangement of components without departing from the spirit and scope of this disclosure. It is understood that the invention is not limited to the embodiments set forth herein for purposes of exemplification, but is to be limited only by the scope of the attached claim or claims, including the full range of equivalency to which each element thereof is entitled.

## Clean Version of the Claims

1. (Amended) A signal sequencing control means for an electronic device, said sequencing control means comprising:

an electronic circuit driven to generate the sequence of control signals in a forward and reverse direction along the same circuit path; and

timing means to allow a sequence of control signals to be activated in a pre-determined order for operation of the device and deactivated in a reverse order for disabling the device.

2. (Amended) A signal sequencing control means according to claim 1 wherein each signal is controlled by a resistor/capacitor combination.

3. (Amended) A signal sequencing control means according to claim 2 wherein the control signals are controlled by a network of said resistor/capacitor combinations and the network provides the activation/deactivation of the signals in sequence at pre-determined time intervals.

4. (Amended) A signal sequencing control means according to claim 3 wherein the resistors of the network are provided in series.

5. (Amended) A signal sequencing control means according to claim 1 wherein said sequence of control signals is being operated via <u>at least one</u> logic.

6. (Amended) A signal sequencing control means according to claim 5 wherein at least one of said logic gate is a Schmidt Logic Gate.

7. (Amended) A signal sequencing control means according to claim 1 wherein the circuit path includes at least one logic gate and voltage is driven by at least one of said gates along a circuit path through a series of resistors in a first direction via a

diode at the start of the resistor path, and a reverse diode being provided at the end of the resistor path to drive the voltage through the resistors in the reverse direction.

8. (Amended) A signal sequencing control means according to claim 1 wherein said sequence of signals in a forwards direction is different to the sequence of signals in a reverse direction and the control signals in the forwards and reverse direction is driven using the same circuit path.

9. (Amended) A signal sequencing control means according to claim 1 wherein said electronic device is a smart card.

10. (Amended) A signal sequencing control means according to claim 9 wherein said smart card has at least three lines which need to be activated in a pre-determined order for operation of said device and deactivated in a reverse order for disabling said device.

11. (Amended) A signal sequencing control means for a smart card interface, said interface comprising:

an electronic circuit driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path; and

timing means to allow a sequence of control signals to be activated in a pre-determined order for operation of the card and deactivated in a reverse order for disabling the card.

12. (Amended) A smart card reading apparatus, said apparatus for reading/receiving and processing signals for a smart card, said reading apparatus comprising:

an electronic circuit driven to generate the sequence of control signals in a forwards and reverse direction along the same circuit path; and a timing means to allow a sequence of control signals to be activated in a pre-determined order for operation of the card and deactivated in a reverse order for disabling the card.